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APPLICATIONS OF JOSEPHSON JUNCTION SQUIDS AND ARRAYS.(U)
JAN 82 A H SILVER N00014-81-C-0615

UNCLASSIFIED NL

FIRST QUARTERLY REPORT

TO THE

OFFICE OF NAVAL RESEARCH
CODE 414
800 N. QUINCY ST.
ARLINGTON, VA 22217

ON

# APPLICATIONS OF JOSEPHSON JUNCTION SQUIDS AND ARRAYS

CONTRACT NO. N00014-81-C-0615



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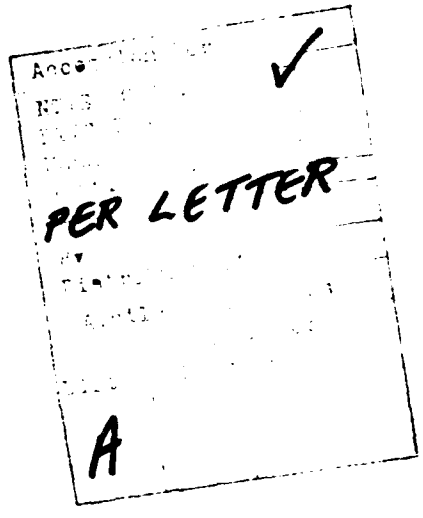
## I. INTRODUCTION

This is the first quarterly progress report for Contract No. N00014-81-C-0615, "Applications of Josephson Junction SQUIDs and Arrays", covering the period from the start date 8 September 1981 through 25 December 1981. It includes the work plan, the status of tasks initiated during this period, and a brief review of related IR&D programs on Josephson technology.



## 2. WORK PLAN

This is a new contract for a projected multi-year investigation of Superconducting QUantum Interference Device (SQUID) arrays and their application to microwave technology. The focus of this contract is the investigation and demonstration of a SQUID voltage-controlled oscillator (VCO). The array is then projected to increase the available power and operating impedance. The approach adopted will utilize monolithic superconducting integrated circuits which will be designed, fabricated, and tested at TRW.

The project has three tasks:

Task 1. Analysis of dc SQUID Arrays;

Task 2. Design of dc SQUID Generator;

Task 3. SQUID VCO Fabrication and Measurement;

which are being carried out, in accordance with the diagram of Figure 1. A number of the steps are very similar to those required for a contract with the Naval Research Laboratory, "Demonstration of a SQUID Parametric Amplifier". Such steps are carried out jointly, and we expect both contracts to benefit from this interaction.

## 3. PROGRESS

### 3.1 Transformer Design

Since the anticipated SQUID VCO is necessarily a very low impedance device, a suitable transformer is an essential ingredient for evaluating the basic VCO, particularly with respect to available power. In order to carry out this transformation in both impedance and dimension in a reproducible and predictable manner, the transformer will be integrated with the active circuitry as proposed.

The basic architecture of the transformer was presented in the contract proposal. We have refined the design for the TRW fabrication process and reconsidered the problems of launching from 50Ω coaxial cable into 50Ω coplanar line, dimensional step from 1 mm coplanar line line at 50Ω, and construction of capacitors in the lumped element impedance transformer. The electrical design was optimized numerically using COMPACT with a computed VSWR < 1.25 over the 8-12 GHz band (Figure 2). Figure 3 shows the equivalent electrical circuit and the geometrical layout.

A test of the effect of changing dimensions in 50Ω coplanar line was performed by fabricating three 50Ω transmission lines: a continuous coplanar line at mm dimensions, a sharply stepped coplanar line, and a short, tapered transition as shown in Figure 4. The measured performance showed no significant differences between the three lines. Therefore, the input LC circuit in the transformer intended to tune out the inductance of the step in the coplanar line was deleted.

The transformer was designed to be fabricated on a 2 inch silicon wafer 0.015 in. thick with a minimum line width of 50μm. An OSM microwave launcher drives the 50Ω coplanar line which has a center conductor width equal to 1.3 mm, a ground plane spacing of 0.4 mm, and an effective dielectric constant of 4.4. The coplanar line is tapered at 50Ω to a center conductor width of 50μm, ground plane spacing of 30μm, and an effective dielectric constant of 6.4. The reduction in ε and its dependence on linewidths results from the finite thickness of the Si substrate. The 1Ω microstrip in the transformer is 50μm wide and separated from the Nb ground plane by 50nm $Nb_2O_5$ and 200nm SiO. It has an effective ε=13.

The transformer design incorporates short ($< \lambda/4$) sections of coplanar and microstrip lines which act as lumped inductors and capacitors, respectively. The inductive lines are 50Ω coplanar lines terminated by 1Ω microstrip, with $L \approx Z_o \ell / v$, where $Z_o$ is the line impedance, $\ell$ the line length, and v the propagation velocity. Capacitors are 1Ω and 0.5Ω microstrip either terminated by 50Ω coplanar or used as open parallel stubs. The capacitance of short, open lines is given by $C \approx \ell / Z_o v$.

Photolithographic patterns were defined as 4-level masks and produced by TRW Microelectronics Center for the combined dimensional and impedance transformer. Circuits will be fabricated and tested in the next quarter. For the dimensions and tolerances required, masks were fabricated directly at the reticle level in an Electromask pattern generator. Figure 5 shows the computer-generated composite of three 1 cm x 2 cm ships which will be fabricated on 2" silicon wafers, 0.15"

thick. Each chip has 2 coplanar inputs with tapered lines. On one chip the reduced width coplanar line couples directly through; on the second chip, transformers from each end are connected for in-out transmission measurements. The third chip has each coplanar line and transformer terminated with a matched resistive load. Figure 6 is an expanded plot of the transformer and terminating resistor on the third chip.

3.2 SQUID Design

The first phase SQUID VCO will be a resistive SQUID driven by the dc voltage developed across the small biasing resistor. The SQUID was designed to utilize the $Nb/Nb_2O_5/PbBi$ junctions used at TRW. The source impedance derived from $\sqrt{L/C}$ is set at 0.3Ω such that the 1Ω transformer load will result in Q=3. The design values are selected by setting the flux quantum energy = $10^4$ kT, producing:

$L = 5$ pH

$C = 65$ pH

$\beta = 1$

$I_c = 67\mu A$

$j_o = 9$ A/cm$^2$

Area = 50 um x 14.9 um = 745 um$^2$.

The biasing resistor r, which should establish the line width, has not been specified at this time. We intend to vary r between $10^{-6}$ and $10^{-3}\Omega$ to recheck the relationship between linewidth and resistance.

3.3 Fabrication

A decision was made to use Si substrates rather than sapphire. Fifty 2" wafers were obtained and the chip size set at 1 cm x 2 cm. Three chips will be cut from one wafer after fabrication. This approach should eliminate problems at the edges of the wafer during fabrication.

Fabrication of resistors in the range of interest, $10^{-6}$ - $10^{3}$ Ω, with usual planar thin films appears to be difficult to achieve reproducibly. We have developed a new concept for an edge resistor which can be controlled in this resistance range. Figure 7 shows the proposed method of fabricating such low impedance resistors. This will be tested during the second quarter.

3.4 Analysis

Analysis of the SQUID VCO was initiated with the idealized SQUID to which the various non-ideal elements such as capacitance, dc voltage source resistance, and load resistance were added. The changes in the differential equations were studied. Then, the voltage-clamped dc SQUID VCO was described and the coupled differential equations derived. These will be solved numerically.

The voltage-clamped dc SQUID can be viewed as two identical resistive SQUIDs coupled with a common biasing resistor. In principle, two other versions of coupled resistive SQUIDs could have common inductors or a common inductor/bias resistor pair. In the former case, there are two bias resistors, an undesirable configuration; in the latter case the resulting configuration appears physically impossible to achieve. Thus, the voltage clamped dc SQUID VCO appears to be the best choice for combining resistive SQUIDs. (Figure 8)

Previous limited analysis of the transverse flow dc SQUID array[1] reported only one dispersion curve for the linearized array described by

$$\omega^2 LC = 2\,(3-\cos k)^{-1}.$$

Since this array has two values for the junction critical current and capacitance, there must be two branches in the dispersion curve. Further inspection showed that the second branch is described by $\omega^2 LC=0$ and

represents zero frequency currents with no current in the inductors of the array. This branch will be of no interest to us.

1. Parametric Properties of SQUID Lattice Arrays, A.H. Silver, D.C. Pridmore-Brown, R.D. Sandell and J.P. Hurrell, IEEE Trans. Mag. MAG-17, 412 (1981).

## 4. RELATED IR&D

TRW conducted 3 IR&D programs in 1981 which involved development of superconducting electronics. The principal accomplishments of interest here were the acquisition and installation of a cryopumped S-Gun magnetron sputtering system for rapid deposition of high quality Nb films, the assembly of an SiO film vacuum deposition system, refinement of lift-off photolithography using chlorobenzene soak and the introduction of a PMM/ Shipley lift-off process for higher resolution lithography, improvement in the processing of $Nb/Nb_2O_5/Pb$-Bi junctions, and initial considerations of a fully digital SQUID sensor and analog Josephson switches for array multiplexing.

5. FINANCIAL

As of 25 December 1981, the total booked cost is $12,863. against a contract cost of $69,055. plus anticipated fees of $5,945. We anticipate expenditures of $65,000. by 30 May 1982, with the remaining $4,055. budgeted for preparing the final report and publication.

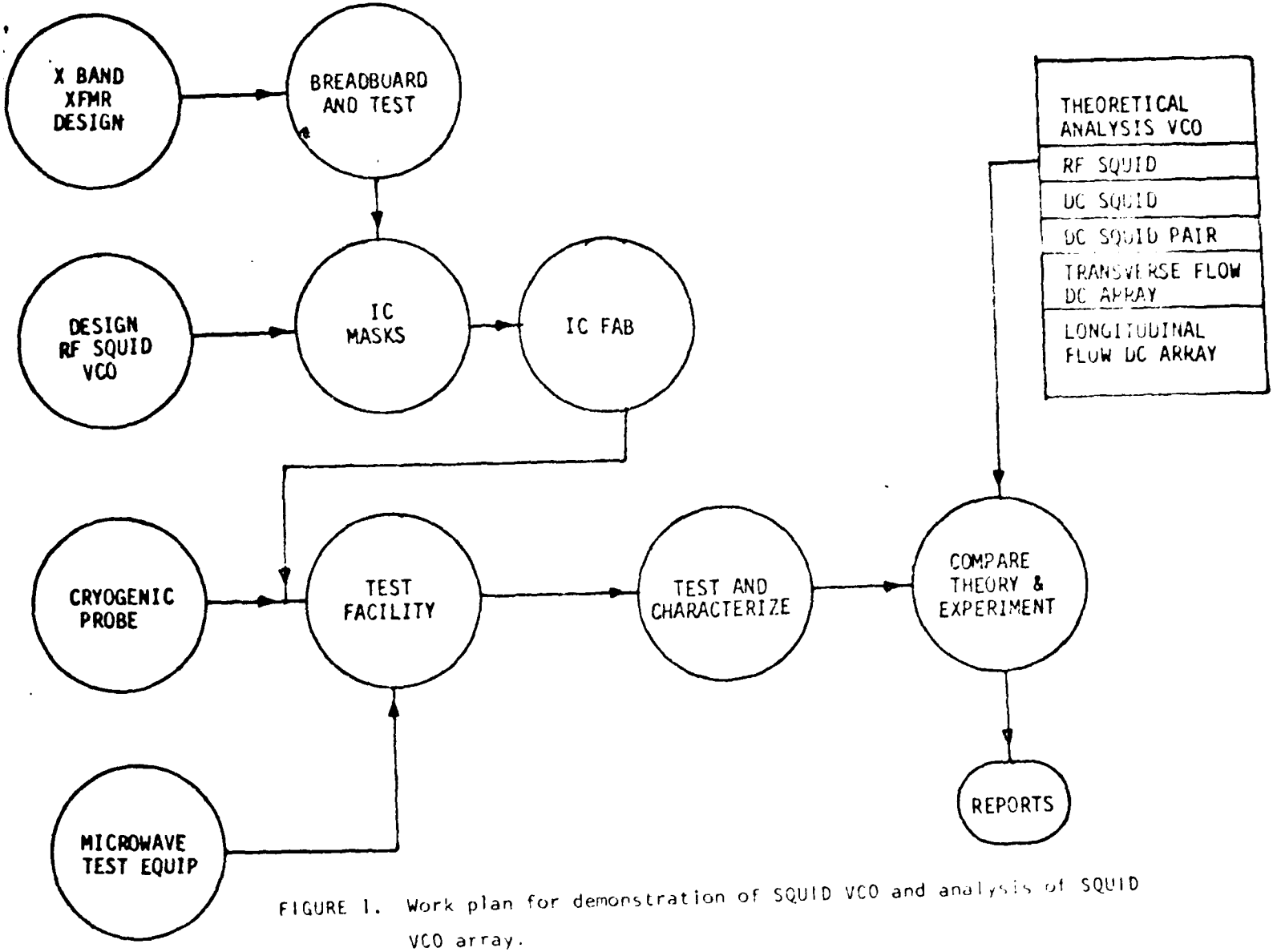



FIGURE 1. Work plan for demonstration of SQUID VCO and analysis of SQUID VCO array.

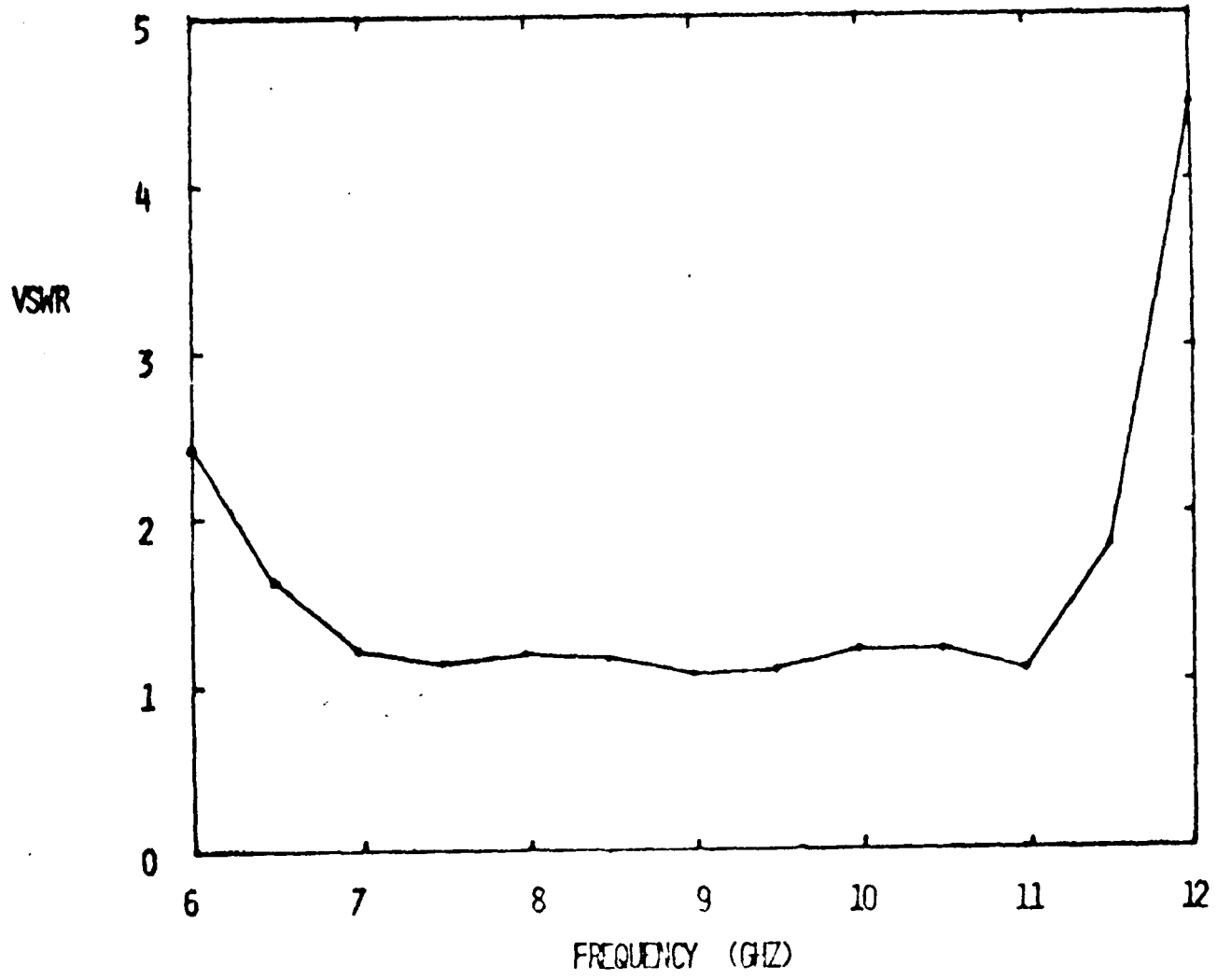



FIGURE 2. Computed voltage standing wave radio (VSWR) as a function of frequency for transformer circuit shown in Figure 3.

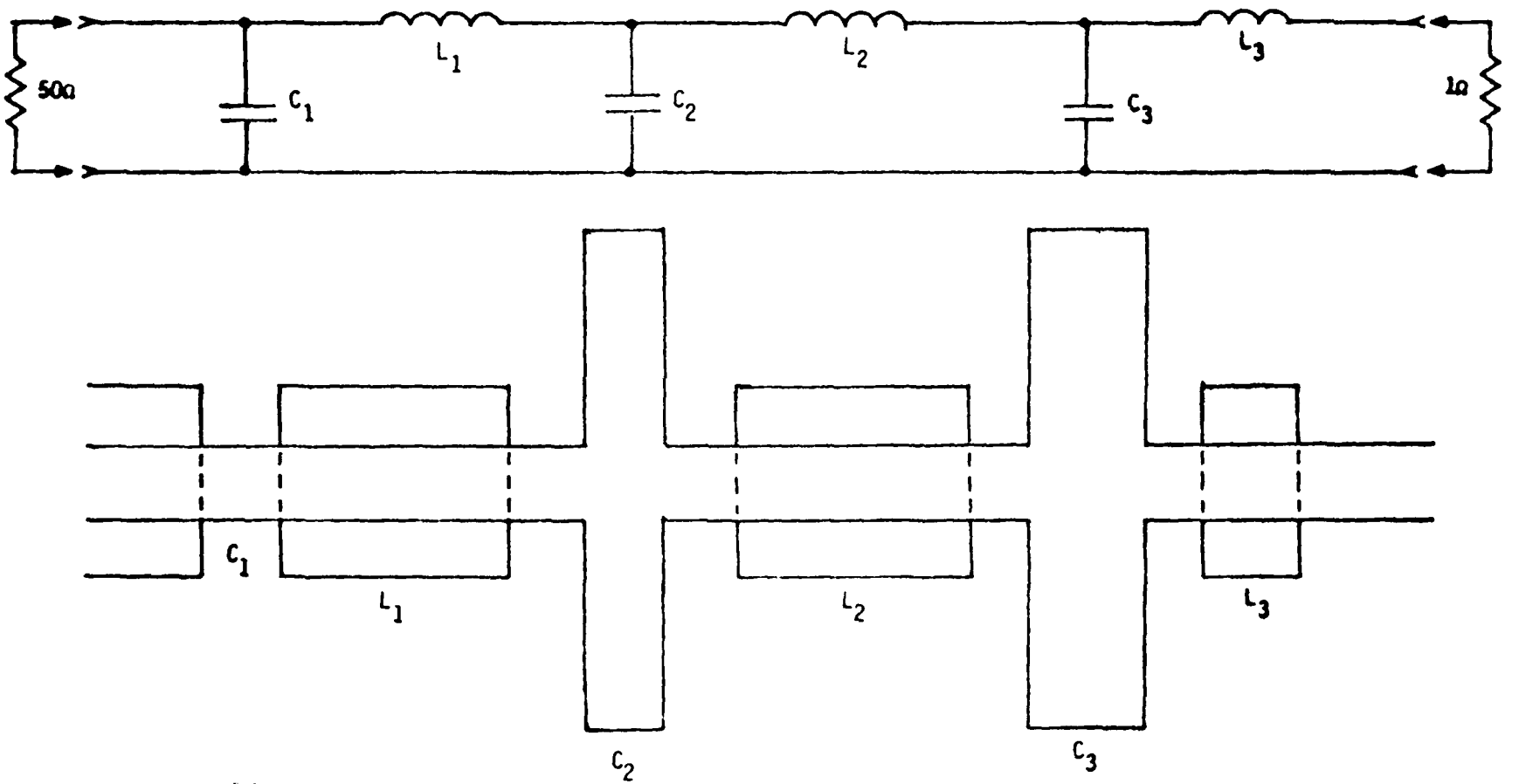



FIGURE 3. Equivalent circuit (top) and physical layout (not to scale) of X-band transformer designed and simulated. The lumped circuit parameters are $C_1$ = 0.6 pF, $L_1$ = 442 pH, $C_2$ = 1.6 pF, $L_2$ = 108 pH, $C_3$ = 8.6 pF, $L_3$ = 22 pH.

FIGURE 4. Photograph of the 50.. coplanar lines used to test dimensional changes.

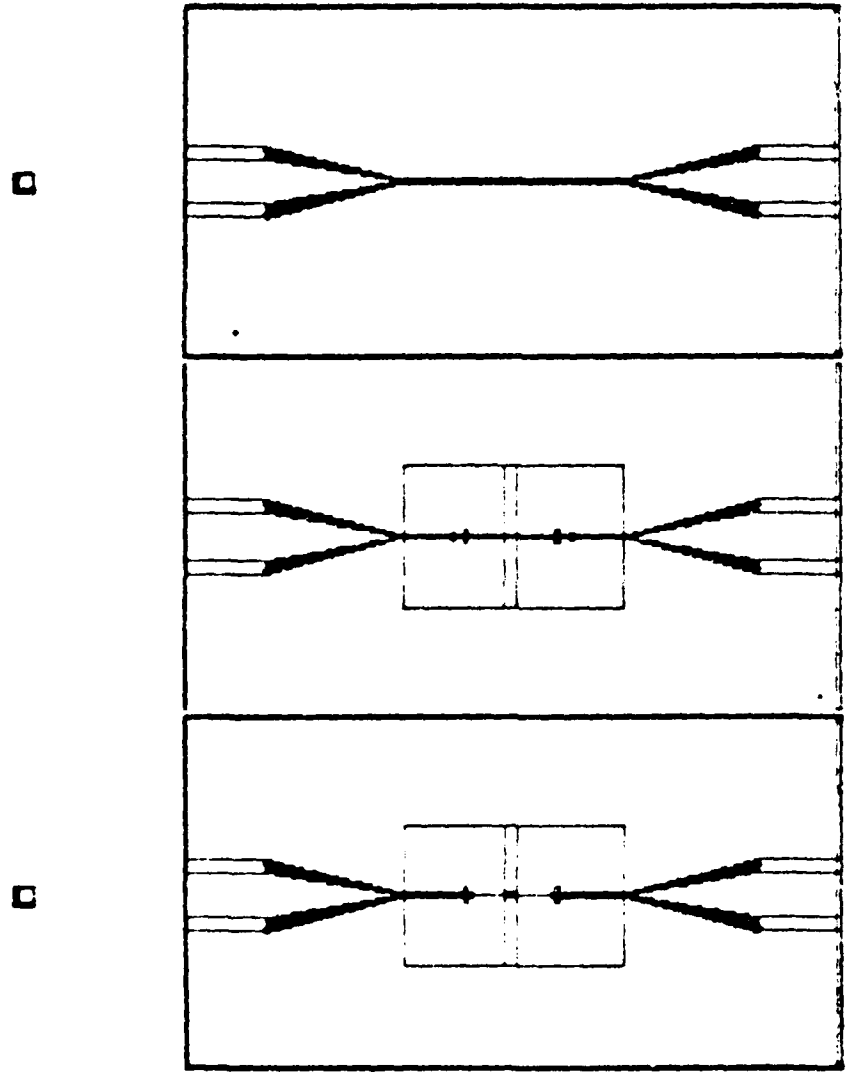


FIGURE 5. Printout of composite masks for the 50Ω to 1Ω transformers. Top: 50Ω stepped coplanar transmission lines; Center: 50Ω coplanar to 1Ω microstrip to 50Ω coplanar line; Bottom: 50Ω coplanar to 1Ω microstrip terminated.

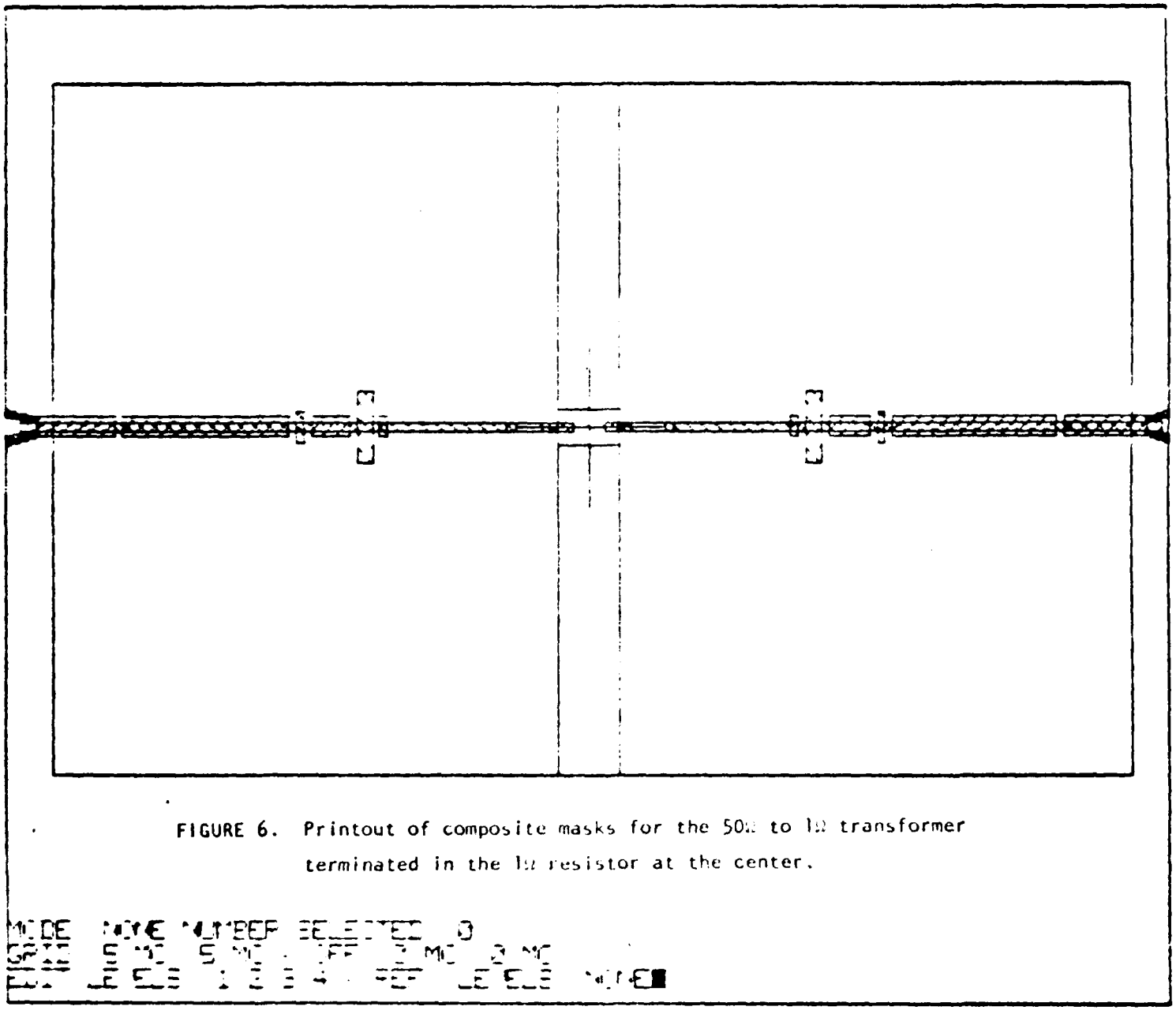


FIGURE 6. Printout of composite masks for the 50Ω to 1Ω transformer terminated in the 1Ω resistor at the center.

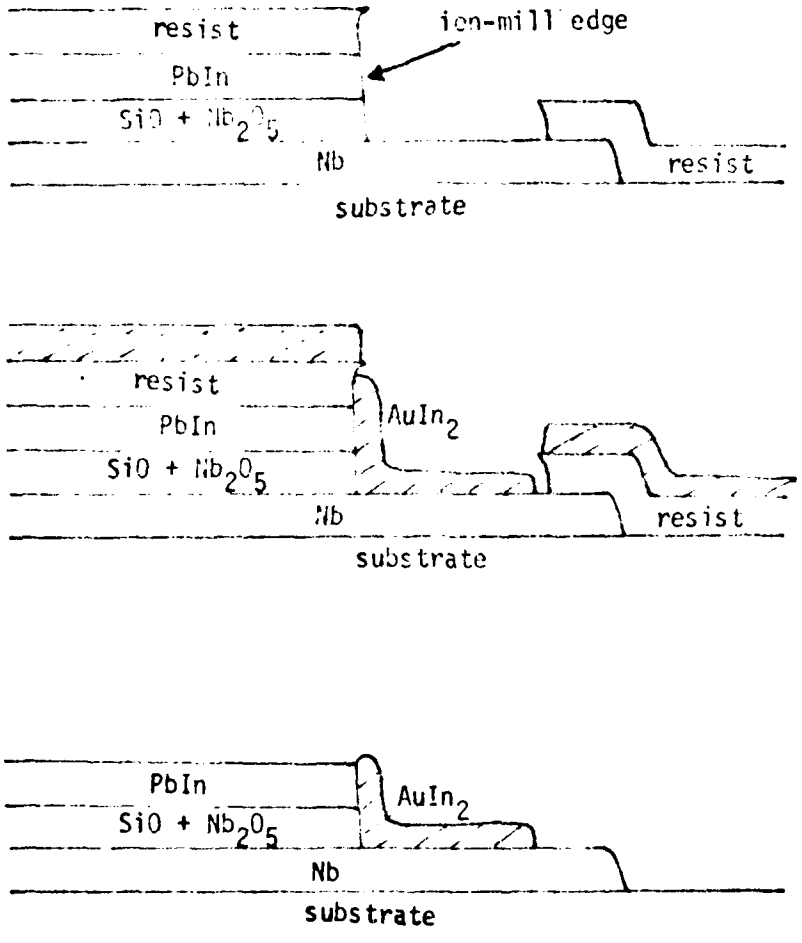



FIGURE 7. Fabrication process for low impedance edge resistor proposed for the VCO.

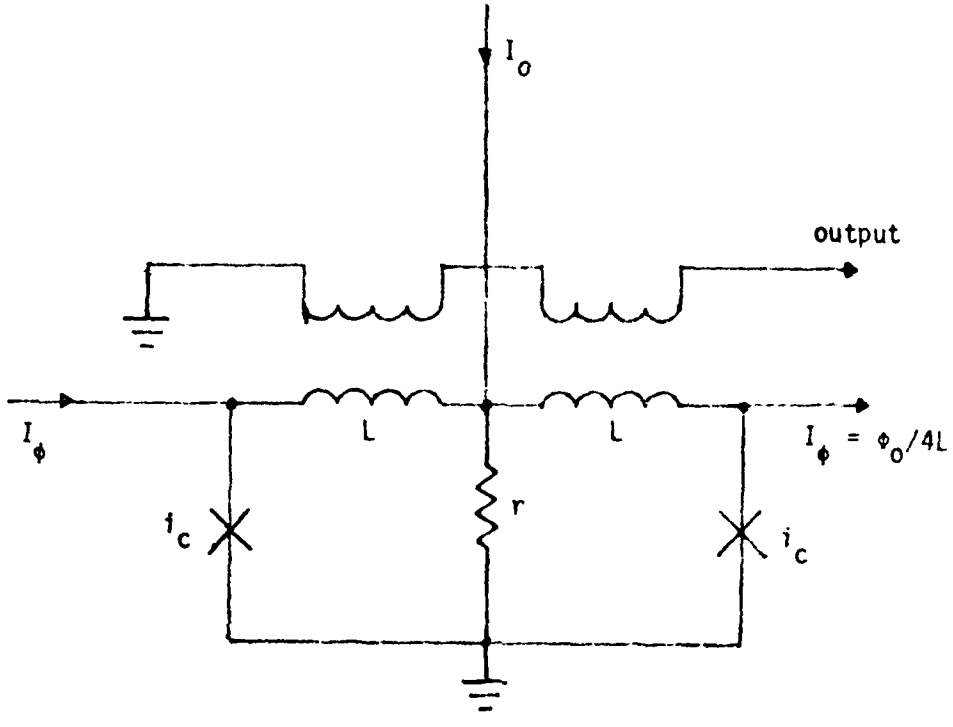
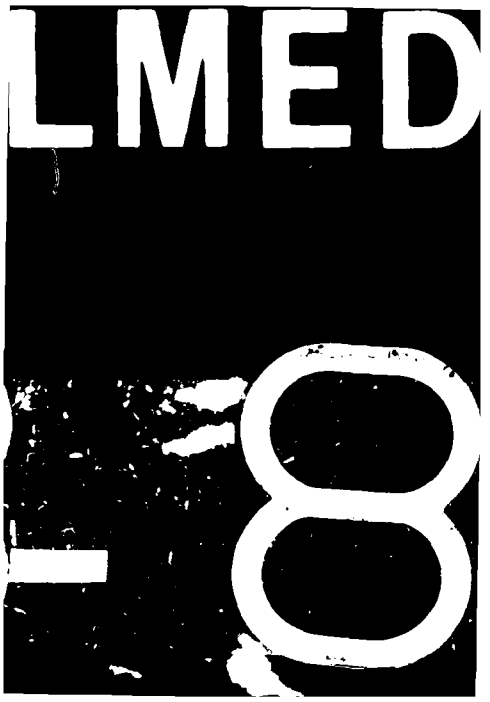



FIGURE 8. Schematic diagram of volyage-clamped dc SQUID VCO.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